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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,265	10/07/2003	Stefan Marinca	T0461.70041US00	6382
23628 7590 11/23/2007 WOLF GREENFIELD & SACKS, P.C. 600 ATLANTIC AVENUE BOSTON, MA 02210-2206			EXAMINER ROSSOSHEK, YELENA	
			ART UNIT 2825	PAPER NUMBER
			MAIL DATE 11/23/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/680,265

Applicant(s)

MARINCA ET AL.

Examiner

Helen Rossoshek

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 September 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8, 17-35, 37 and 38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 17-35, 37 and 38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the Application 10/680,265 filed 10/07/2003 and amendment filed 09/10/2007.

2. Claims 1-8, 17-35, 37 and 38 remain pending in the Application. Claim 36 has been canceled from the Application. Claim 38 has been added to the Application.

3. Applicant's arguments have been fully considered and they are partly persuasive. However, upon further consideration, a new ground(s) of rejection is made in view of Nolan et al. (US Patent 6,356,161).

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claim 38 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims are drawn to a computer program per se. A computer program per se is abstract instructions. Therefore, a computer program is not a physical thing (product) nor a process as they are not "acts" being performed. As such, these claims are not directed to one of the statutory categories of invention (See MPEP 2106.01), but are directed to nonstatutory functional descriptive material.

It is noted that computer programs embodied on a computer readable medium or other structure, which would permit the functionality of the program to be realized, would be directed to a product and be within a statutory category of invention, so long as the

computer readable medium is not disclosed as non-statutory subject matter per se (signals or carrier waves).

Therefore in response to the Applicant's arguments on the pages 8-9 of the amendment filed 09/10/2007 should be noted that claimed "transmitting signal" is not permissible (See MPEP 2106.01):

When nonfunctional descriptive material is recorded on some computer-readable medium, in a computer or on an electromagnetic carrier signal, it is not statutory and should be rejected under 35 U.S.C. 101. In addition, USPTO personnel should inquire whether there should be a rejection under 35 U.S.C. 102 or 103. USPTO personnel should determine whether the claimed nonfunctional descriptive material be given patentable weight. USPTO personnel must consider all claim limitations when determining patentability of an invention over the prior art. In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 403-04 (Fed. Cir. 1983). USPTO personnel may not disregard claim limitations comprised of printed matter. See Gulack, 703 F.2d at 1384, 217 USPQ at 403; see also Diehr, 450 U.S. at 191, 209 USPQ at 10. However, USPTO personnel need not give patentable weight to printed matter absent a new and unobvious functional relationship between the printed matter and the substrate. See In re Lowry, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994); In re Ngai, 367 F.3d 1336, 70 USPQ2d 1862 (Fed. Cir. 2004).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8, 17-35, 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Nolan et al. (US Patent 6,356,161).

With respect to claim 1 Nolan et al. teaches a method for compensating for temperature effects during operation of a semiconductor circuit (abstract) comprising:

scaling an output voltage value of the circuit to a desired output value at a first temperature (within a bandgap reference voltage circuit 150 shown on the Fig. 3 to produce a reference voltage 152 (col. 3, ll.9-11; col. 5, ll.18-20), wherein the reference voltage 152 might be produces/scaled by various of the reference voltage circuits 150 (col. 5, ll.59-67)); and

altering the temperature of the circuit from the first temperature to a second temperature and correcting the output value at the second temperature to match the desired output value, whereby the correction to provide the desired output value at the second temperature does not change the output value at the first temperature (within computing temperature coefficient including current measurements at two distinct temperatures (col. 3, ll.11-14; ll.50-58), wherein independent current calibration method allows to set CTAT current to a predetermined value at a nominal temperature and PTAT current to set to zero and alternatively: to set PTAT current to a predetermined value at a nominal temperature and CTAT current to set to zero (col. 3, ll.14-20; col. 4, ll.63-67; col. 5, ll.1-5));

With respect to claim 17 Nolan et al. teaches the limitations similar to the limitations of the claim 1 including a semiconductor circuit adapted to provide compensation for temperature effects during operation (within circuit shown o the Fig. 3; abstract; col.1, ll.65-67; col. 2,ll,1-3)).

With respect to claim 31 Marinca teaches a semiconductor circuit adapted to provide compensation for temperature effects during operation (within circuit shown o the Fig. 3; abstract; col.1, ll.65-67; col. 2,ll,1-3)), the circuit comprising:

a digital control means for: digitally scaling an output voltage of said circuit to a desired output voltage value at a first temperature (within a bandgap reference voltage circuit 150 shown on the Fig. 3 to produce a reference voltage 152 (col. 3, ll.9-11; col. 5, ll.18-20), wherein the reference voltage 152 might be produces/scaled by various of the reference voltage circuits 150 (col. 5, ll.59-67), wherein the process of trimming the current is performed digitally (col. 6, ll.44-48)); and

digitally matching said output voltage value, at a second temperature, to said desired output voltage value, whereby said desired output voltage value at said first temperature remains unchanged (within computing temperature coefficient including current measurements at two distinct temperatures (col. 3, ll.11-14; ll.50-58), wherein independent current calibration method allows to set CTAT current to a predetermined value at a nominal temperature and PTAT current to set to zero and alternatively: to set PTAT current to a predetermined value at a nominal temperature and CTAT current to set to zero (col. 3, ll.14-20; col. 4, ll.63-67; col. 5, ll.1-5), wherein the process of trimming the current is performed digitally (col. 6, ll.44-48)).

With respect to claim 35 Nolan et al. teaches a computer program product comprising a tangible, computer-readable medium having embodied therein program instructions for causing a computer to perform the method of claim 1, when executed (within CPU 900 shown on the Figs. 7-10 coupled to a memory (col. 8, ll.29-31)).

With respect to claims 2-8, 18-30 and 32-37 Nolan et al. teaches:

Claim 2: wherein the step of scaling the output value is effected by the addition or subtraction of a constant voltage value (col. 7, ll.21-24; col. 5, ll.13-14; col. 10, ll.61-67; col. 11, ll.1-5);

Claims 3, 19: wherein the constant voltage value is generated by forcing a constant current through a resistor of the circuit (col. 6, ll.36-40; 60-64);

Claim 4: comprising generating the current from a balanced combined PTAT and CTAT current (col.5, ll.3-13);

Claim 5: comprising generating the current from reflecting a reference voltage across the resistor (col. 6, ll.25-39);

Claims 6, 23: wherein the matching step is effected by the addition or subtraction of the difference between two balanced trimming PTAT and CTAT currents (col. 3, ll.15-21);

Claims 7, 24: wherein the trimming currents are such that at the first temperature the difference between each current is zero and the combined current value has a double slope compared to a slope value of each individual current (col. 10, ll.26-37);

Claims 8, 26: between the scaling and the matching step, comprising the additional step of tuning of the trimming currents such that the difference between the PTAT and CTAT currents at the first temperature is equal to zero (col. 6, ll.44-50);

Claim 18: wherein the means for scaling the output comprises a multiplexor for adding or subtracting the output by a constant value (col. 6, ll.49-52);

Claim 30: wherein the values of the trimming currents providing the difference are stored in memory (col.);

Claim 36: wherein the medium includes a read-only memory (col. 8, ll.29-31).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 20-22, 25, 27-29, 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan et al. as applied to claims 17 and 31 above, and further in view of Dauphinee et al. (US Patent 7,068,100).

With respect to claims 20-22, 25, 27-29, 32-34 Nolan et al. teaches the limitations, from which the claims depend. Nolan et al. disclose decoder shown on the Fig. 1 for controlling the ratio of PTAT current and CTAT current, however Nolan et al.

lacks specifics regarding controlling the constant current by a current source coupled to a DAC. Dauphinee et al. teaches:

Claim 20: wherein the value of the constant current is controlled by a current source coupled to DAC, a value of a user controlled input code applied to the DAC to determine the value of the constant current (col. 17, ll.27-40; Fig. 16A);

Claim 21: wherein the addition or subtracting of the constant voltage value is controlled by at least one of the multiplexors coupled to two outputs of the DAC, to determine whether the constant voltage value is to be added or subtracted (col. 17, ll.27-40; Fig. 16A);

Claim 22: wherein the addition or subtracting of the constant voltage value is controlled by a second input to the DAC (col. 17, ll.27-40; Fig. 16A);

Claim 25: wherein the PTAT and CTAT trimming currents are controlled by a first and second DAC, the output of the first and second DAC connected to at least one multiplexor, whereby a control signal applied to the multiplexor controls the addition or subtraction of the difference (col. 18, ll.54-67);

Claim 27: wherein the tuning means comprises a tuning DAC coupled to a source of one of the currents, such that tuning may be achieved by adjusting a value of a user controlled input to the tuning DAC (col. 19, ll.1-17);

Claim 32: wherein a constant current is generated by a balanced combination of PTAT and CTAT current sources, each current source coupled to a DAC, the value of an input code applied to an input of each DAC determining the value of the constant

current, and wherein the addition or subtracting of the constant voltage value is controlled by a second input to each DAC (col. 19, ll.18-27);

Claim 33: wherein the digital control means comprises register, coupled to the inputs of each DAC, wherein the output values from the register determine the value of the input codes to each DAC (col. 19, ll.8-12);

With respect to claim 34 Nolan et al. teaches:

Claim 34: wherein the register is connected to a digital control unit and memory, the value of the input codes are stored in the memory, and the transfer of the input codes from memory to the register is controlled by the digital control unit (col. 2, ll.60-67; col. 3, ll.1-5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Dauphinee et al. to teach specifics Nolan et al. does not teach, because it is implemented more linear, lower noise, less costly amplifier assembly for providing variable amplifier gain in a variety of applications, such as those including multiple tuners for cable television and data signal applications (col. 1, ll.27-30).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
11/20/2007

Examiner Helen Rossoshek
/Helen Rossoshek/
Art Unit 2825